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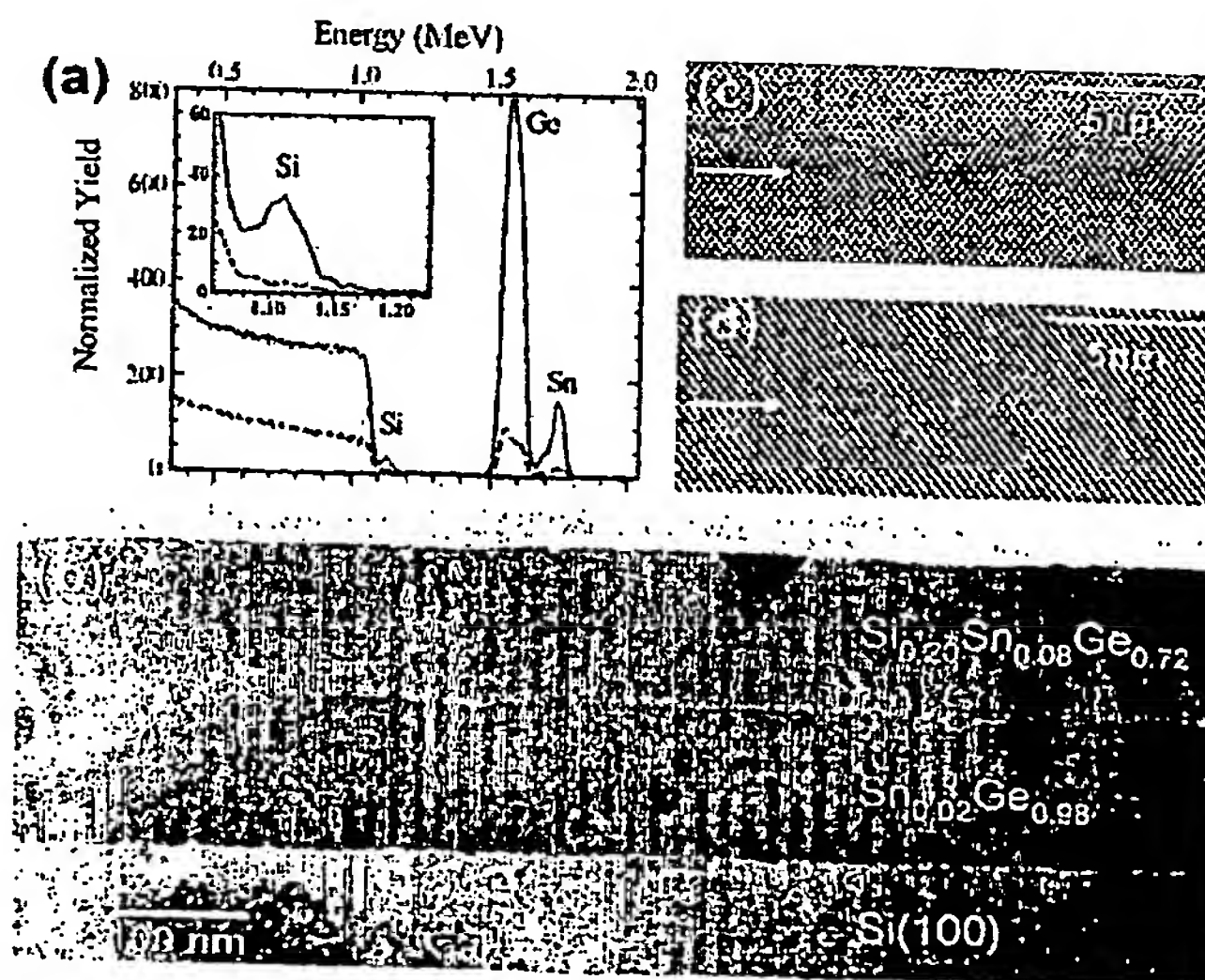
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[Continued on next page]

(54) Title: **Si<sub>x</sub>Sn<sub>y</sub>Ge<sub>1-x-y</sub> AND RELATED ALLOY HETEROSTRUCTURES BASED ON SI, GE AND SN**



(57) Abstract: A novel method for synthesizing device-quality alloys and ordered phases in a Si-Ge-Sn system uses a UHV-CVD process and reactions of SnD<sub>4</sub> with SiH<sub>3</sub>GeH<sub>3</sub>. Using the method, single-phase Si<sub>x</sub>Sn<sub>y</sub>Ge<sub>1-x-y</sub> semiconductors (x ≤ 0.25, y ≤ 0.11) are grown on Si via Ge<sub>1-x</sub>Sn<sub>x</sub> buffer layers. The Ge<sub>1-x</sub>Sn<sub>x</sub> buffer layers facilitate heteroepitaxial growth of the Si<sub>x</sub>Sn<sub>y</sub>Ge<sub>1-x-y</sub> films and act as compliant templates that can conform structurally and absorb the differential strain imposed by the more rigid Si and Si-Ge-Sn materials. The SiH<sub>3</sub>GeH<sub>3</sub> species was prepared using a new and high yield method that provided high purity semiconductor grade material.

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WO 2005/015609 A2



**Declarations under Rule 4.17:**

- *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii)) for the following designations AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW, ARIPO patent (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE,*

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- *of inventorship (Rule 4.17(iv)) for US only*

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